PENDING CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

1-6. (Canceled)

7. (Previously Amended) A method comprising performing the steps in the order presented:

supplying an input bit stream to a channel coding block;

modulating an output of the channel coding block to provide a modulation symbol sequence and frequency coding the modulation symbol sequence;

feeding a replica of the entire frequency coded modulation symbol sequence to each of a plurality of orthogonal sequence covers, wherein each of the plurality of orthogonal sequence covers outputs one of a plurality of spread sequences of output chips;

performing inverse Fast Fourier Transform (FFT) and cyclic prefix processing on the plurality of spread sequences of output chips to yield a plurality of outputs; and

transmitting the plurality of outputs over a multiple-input multiple-output channel.

8. (Previously Presented) A method comprising:

supplying an input bit stream to a coding block;

modulating an output of the coding block to provide a first modulation symbol sequence;

diversity encoding the first modulation symbol sequence to generate a second modulation symbol sequence; and

feeding the second modulation symbol sequence to a plurality of orthogonal sequence covers, wherein each of the plurality of orthogonal sequence covers outputs one of a plurality of spread sequences of output chips, and further wherein the plurality of spread sequences of output chips are transmitted over a multiple-input multiple-output channel.

9. (Original) The method of claim 8 wherein the diversity encoding is space-time encoding.

10. (Original) The method of claim 8 wherein the diversity encoding is space-frequency encoding.

11. (Original) The method of claim 8 wherein the feeding step comprises feeding a replica of the second modulation symbol sequence to a pair of the plurality of orthogonal sequence covers.

12. (Canceled)

13. (Original) The method of claim 8 wherein the plurality of orthogonal sequence covers comprise pairwise mutually orthogonal Walsh covers.

14. (Original) The method of claim 8 wherein the modulating step comprises modulating the output of the coding block using trellis coded quadrature amplitude modulation.

15. (Previously Amended) The method of claim 8 further comprising:

frequency coding the modulation symbol sequence after the modulating step and before the feeding step; and

performing inverse Fast Fourier Transform (FFT) and cyclic prefix processing after the feeding step and before the plurality of spread sequences of output chips are

transmitted.

16-22. (Canceled)

23. (Previously Presented) A wireless apparatus comprising:

a coding block configured to encode an input bit stream;

a modulator configured to receive an output of the coding block to provide a first modulation symbol sequence;

an Alamouti block configured to diversity encode the first modulation symbol sequence to generate a second modulation symbol sequence; and

a plurality of orthogonal sequence covers, wherein the second modulation symbol sequence is fed to the plurality of orthogonal sequence covers and each of the plurality of orthogonal sequence covers outputs one of a plurality of spread sequences of output chips, and further wherein the plurality of spread sequences of output chips are queued for transmission over a multiple-input multiple-output channel.

24. (Original) The wireless apparatus of claim 23 wherein the Alamouti block is configured to diversity encode using space-time encoding.

25. (Original) The wireless apparatus of claim 23 wherein the Alamouti block is configured to diversity encode using space-frequency encoding.

26. (Original) The wireless apparatus of claim 23 wherein a replica of the second modulation symbol sequence is fed to a pair of the plurality of orthogonal sequence covers.

27. (Canceled)

28. (Original) The wireless apparatus of claim 23 wherein the plurality of orthogonal sequence covers comprises pairwise mutually orthogonal Walsh covers.

29. (Previously Amended) The wireless apparatus of claim 23 wherein the modulator is configured to modulate the output of the coding block using trellis coded quadrature amplitude modulation.

30-39 (Canceled)

40. (Withdrawn) A method for increasing bandwidth efficiency comprising:

performing Fast Fourier Transform (FFT) and cyclic prefix processing on a plurality of input chip sequences to generate a plurality of output chip sequences;

feeding the plurality of output chip sequences to each of a plurality of orthogonal sequence decovers to yield a plurality of first symbol sequences;

diversity decoding the plurality of first symbol sequences to generate a plurality of second symbol sequences; and

generating a plurality of metrics based on the plurality of second symbol sequences.

41. (Withdrawn) The method of claim 40 further comprising frequency decoding and demodulating the plurality of second symbol sequences responsive to the plurality of metrics.

42. (Withdrawn) The method of claim 41 wherein the plurality of second symbol sequences represents replicas of a single sequence of source symbols at a transmitter.

43. (Withdrawn) The method of claim 42 further comprising receiving the plurality of input chip sequences from the transmitter.

44. (Withdrawn) The method of claim 43 wherein the plurality of second symbol sequences represents a plurality of transmitter symbol sequences which were time-demultiplexed from a single sequence of source symbols at the transmitter.

45. (Withdrawn) The method of claim 40 wherein the diversity decoding is space-time decoding.

46. (Withdrawn) The method of claim 40 wherein the diversity decoding is space-frequency decoding.

47. (Withdrawn) The method of claim 41 wherein the plurality of orthogonal sequence decovers comprises a pairwise mutually orthogonal Walsh decovers.

48. (Withdrawn) The method of claim 41 wherein the feeding step comprises feeding a replica of an entire output chip sequence to a pair of the plurality of orthogonal sequence decovers.

49. (Withdrawn) The method of claim 48 further comprising using trellis decoding for demodulating the plurality of second symbol sequences.

50. (Withdrawn) An apparatus for increasing bandwidth efficiency comprising:

means for performing Fast Fourier Transform (FFT) and cyclic prefix processing on a plurality of input chip sequences to generate a plurality of output chip sequences;

means for feeding the plurality of output chip sequences to each of a plurality of orthogonal sequence decovers to yield a plurality of first symbol sequences;

means for diversity decoding the plurality of first symbol sequences to generate a plurality of second symbol sequences; and

means for generating a plurality of metrics based on the plurality of second symbol sequences.

51. (Withdrawn) The apparatus of claim 50 further comprising means for frequency decoding and demodulating the plurality of second symbol sequences responsive to the plurality of metrics.

52. (Withdrawn) The apparatus of claim 51 wherein the plurality of second symbol sequences represents replicas of a single sequence of source symbols at a transmitter.

53. (Withdrawn) The apparatus of claim 52 further comprising means for receiving the plurality of input chip sequences from the transmitter.

54. (Withdrawn) The apparatus of claim 53 wherein the plurality of second symbol sequences represents a plurality of transmitter symbol sequences which were time-demultiplexed from a single sequence of source symbols at the transmitter.

55. (Withdrawn) The apparatus of claim 50 wherein the diversity decoding is space-time decoding.

56. (Withdrawn) The apparatus of claim 50 wherein the diversity decoding is space-frequency decoding.

57. (Withdrawn) The apparatus of claim 51 wherein the plurality of orthogonal sequence decovers comprises a pairwise mutually orthogonal Walsh decovers.

58. (Withdrawn) The apparatus of claim 51 further comprising means for feeding a replica of an entire output chip sequence to a pair of the plurality of orthogonal sequence decovers.

59. (Withdrawn) The apparatus of claim 58 further comprising means for using trellis decoding for demodulating the plurality of second symbol sequences.

60. (Withdrawn) An apparatus for increasing bandwidth efficiency, the apparatus comprising a processor and a memory, the memory containing program code executable by the processor for performing the following:

performing Fast Fourier Transform (FFT) and cyclic prefix processing on a plurality of input chip sequences to generate a plurality of output chip sequences;

feeding the plurality of output chip sequences to each of a plurality of orthogonal sequence decovers to yield a plurality of first symbol sequences;

diversity decoding the plurality of first symbol sequences to generate a plurality of second symbol sequences; and

generating a plurality of metrics based on the plurality of second symbol sequences.

61. (Withdrawn) The apparatus of claim 60 wherein the memory further comprising program code for frequency decoding and demodulating the plurality of second symbol sequences responsive to the plurality of metrics.

62. (Withdrawn) The apparatus of claim 61 wherein the plurality of second symbol sequences represents replicas of a single sequence of source symbols at a transmitter.

63. (Withdrawn) The apparatus of claim 62 wherein the memory further comprising program code for receiving the plurality of input chip sequences from the transmitter.

64. (Withdrawn) The apparatus of claim 63 wherein the plurality of second symbol sequences represents a plurality of transmitter symbol sequences which were time-demultiplexed from a single sequence of source symbols at the transmitter.

65. (Withdrawn) The apparatus of claim 60 wherein the diversity decoding is space-time decoding.

66. (Withdrawn) The apparatus of claim 60 wherein the diversity decoding is space-frequency decoding.

67. (Withdrawn) The apparatus of claim 61 wherein the plurality of orthogonal sequence decovers comprises a pairwise mutually orthogonal Walsh decovers.

68. (Withdrawn) The apparatus of claim 61 wherein the memory further comprising program code for feeding a replica of an entire output chip sequence to a pair of the plurality of orthogonal sequence decovers.

69. (Withdrawn) The apparatus of claim 68 wherein the memory further comprising program code for using trellis decoding for demodulating the plurality of second symbol sequences.

70. (Withdrawn) A computer-readable medium storing a computer program, wherein execution of the computer program is for:

performing Fast Fourier Transform (FFT) and cyclic prefix processing on a plurality of input chip sequences to generate a plurality of output chip sequences;

feeding the plurality of output chip sequences to each of a plurality of orthogonal sequence decovers to yield a plurality of first symbol sequences;

diversity decoding the plurality of first symbol sequences to generate a plurality of second symbol sequences; and

generating a plurality of metrics based on the plurality of second symbol sequences.

71. (Withdrawn) The computer-readable medium of claim 70 wherein execution of the computer program is also for frequency decoding and demodulating the plurality of second symbol sequences responsive to the plurality of metrics.

72. (Withdrawn) The computer-readable medium of claim 71 wherein the plurality of second symbol sequences represents replicas of a single sequence of source symbols at a transmitter.

73. (Withdrawn) The computer-readable medium of claim 72 wherein execution of the computer program is also for receiving the plurality of input chip sequences from the transmitter.

74. (Withdrawn) The computer-readable medium of claim 73 wherein the plurality of second symbol sequences represents a plurality of transmitter symbol sequences which were time-demultiplexed from a single sequence of source symbols at the transmitter.

75. (Withdrawn) The computer-readable medium of claim 70 wherein the diversity decoding is space-time decoding.

76. (Withdrawn) The computer-readable medium of claim 70 wherein the diversity decoding is space-frequency decoding.

77. (Withdrawn) The computer-readable medium of claim 71 wherein the plurality of orthogonal sequence decovers comprises a pairwise mutually orthogonal Walsh decovers.

78. (Withdrawn) The computer-readable medium of claim 71 wherein execution of the computer program is also for feeding a replica of an entire output chip sequence to a pair of the plurality of orthogonal sequence decovers.

79. (Withdrawn) The computer-readable medium of claim 78 wherein execution of the computer program is also for using trellis decoding for demodulating the plurality of second symbol sequences.

80. (Withdrawn) An apparatus for increasing bandwidth efficiency comprising:
a Fast Fourier Transformer for performing Fast Fourier Transform (FFT) and cyclic prefix processing on a plurality of input chip sequences to generate a plurality of output chip sequences and for feeding the plurality of output chip sequences to each of a plurality of orthogonal sequence decovers to yield a plurality of first symbol sequences;

a diversity decoder for diversity decoding the plurality of first symbol sequences to generate a plurality of second symbol sequences; and

a metric generator for generating a plurality of metrics based on the plurality of second symbol sequences.

81. (Previously Presented) A method for increasing bandwidth efficiency comprising:

supplying an input bit stream to a coding block to generate an output;

modulating the output to provide a first modulation symbol sequence;

diversity encoding a plurality of time-demultiplexed portions of the first modulation symbol sequence to generate a plurality of portions of a second modulation symbol sequence; and

feeding the plurality of portions to a plurality of orthogonal sequence covers, wherein each of the plurality of orthogonal sequence covers generates a spread sequence.

82. (Previously Presented) The method of claim 81 wherein the spread sequence from each of the plurality of orthogonal sequence covers forms a plurality of spread sequences.

83. (Previously Presented) The method of claim 82 further comprising transmitting the plurality of spread sequences over a multiple-input multiple-output (MIMO) channel.

84. (Previously Presented) The method of claim 81 wherein the diversity encoding is space-time encoding.

85. (Previously Presented) The method of claim 81 wherein the diversity encoding is space-frequency encoding.

86. (Previously Presented) The method of claim 82 wherein the feeding step comprises feeding a distinct portion of the second modulation symbol sequence to a pair of the plurality of orthogonal sequence covers.

87. (Previously Presented) The method of claim 82 wherein the plurality of orthogonal sequence covers comprises a pairwise mutually orthogonal Walsh cover.

88. (Previously Presented) The method of claim 82 wherein the modulating step comprises modulating the output of the coding block using trellis coded quadrature amplitude modulation.

89. (Currently Amended) The method of claim 88 wherein the trellis coded quadrature amplitude modulation is of a rate (n-1)/n, wherein n is the number of bits of the output.

90. (Previously Presented) The method of claim 83 further comprising:

frequency coding the first modulation symbol sequence; and

performing an inverse Fast Fourier Transform (FFT) and a cyclic prefix processing on the plurality of spread sequences.

91. (Previously Presented) An apparatus for increasing bandwidth efficiency comprising:

means for supplying an input bit stream to a coding block to generate an output;

means for modulating the output to provide a first modulation symbol sequence;

means for diversity encoding a plurality of time-demultiplexed portions of the first modulation symbol sequence to generate a plurality of portions of a second modulation symbol sequence; and

means for feeding the plurality of portions to a plurality of orthogonal sequence covers, wherein each of the plurality of orthogonal sequence covers generates a spread sequence.

92. (Previously Presented) The apparatus of claim 91 wherein the spread sequence from each of the plurality of orthogonal sequence covers forms a plurality of spread sequences.

93. (Previously Presented) The apparatus of claim 92 further comprising means for transmitting the plurality of spread sequences over a multiple-input multiple-output (MIMO) channel.

94. (Previously Presented) The apparatus of claim 91 wherein the diversity encoding is space-time encoding.

95. (Previously Presented) The apparatus of claim 91 wherein the diversity encoding is space-frequency encoding.

96. (Currently Amended) The apparatus of claim 92 wherein the means for feeding ~~step comprises~~ is further configured for feeding a distinct portion of the second modulation symbol sequence to a pair of the plurality of orthogonal sequence covers.

97. (Previously Presented) The apparatus of claim 92 wherein the plurality of orthogonal sequence covers comprises a pairwise mutually orthogonal Walsh cover.

98. (Currently Amended) The apparatus of claim 92 wherein the means for modulating ~~step comprises~~ is further configured for modulating the output of the coding block using trellis coded quadrature amplitude modulation.

99. (Currently Amended) The apparatus of claim 98 wherein the trellis coded quadrature amplitude modulation is of a rate (n-1)/n, wherein n is the number of bits of the output.

100. (Previously Presented) The apparatus of claim 93 further comprising:

means for frequency coding the first modulation symbol sequence; and

means for performing an inverse Fast Fourier Transform (FFT) and a cyclic prefix processing on the plurality of spread sequences.

101-120. (Canceled)

121. (Currently Amended) An apparatus for increasing bandwidth efficiency comprising:

a bit stream supplier for supplying an input bit stream to a coding block to generate an output;

a modulator for modulating the output to provide a first modulation symbol sequence; and

a diversity encoder for diversity encoding a plurality of time-demultiplexed portions of the first modulation symbol sequence to generate a plurality of portions of a second modulation symbol sequence; and ~~for feeding the plurality of portions to a plurality of orthogonal sequence covers~~

a plurality of orthogonal sequence covers for receiving the plurality of portions of the second modulation symbol sequence, wherein each of the plurality of orthogonal sequence covers generates a spread sequence.

122. (Previously Presented) The apparatus of claim 121 further comprising:

a frequency coder for frequency coding the first modulation symbol sequence; and

an inverse Fast Fourier Transform (FFT) for performing an inverse FFT and a cyclic prefix processing on the plurality of spread sequences.